A 1V Monolithic Transformer-Coupled 30-Gb/s 2:1 Multiplexer in 120 nm CMOS

Student paper

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Abstract **A completely integrated transformer coupled 2:1 multiplexer for high speed operation in 0.12μm standard CMOS is presented. The multiplexer uses a monolithic transformer to couple the clock to the multiplexer core. This circuit technique allows the 2:1 multiplexer to work from a single 1 V supply voltage while achieving data rates of 30 Gb/s.**

I. Introduction

A key block in high-speed data communication systems is a parallel-to-serial data multiplexer (MUX). Current 2:1 MUX already achieve operating speeds of 25 Gb/s in CMOS [1]. Complete transmitter/receiver with integrated 16:1 MUX/DEMUX in CMOS has been published [2], [3]. On-chip transformers are used successfully for mixer circuits [4] and power amplifiers [5], [6]. In this work a monolithic transformer is used in a high-speed MUX circuit to achieve 30 Gb/s operation at 1 V supply voltage.

Communication systems at bit rates of 40 Gb/s are dominated by technologies such as SiGe, GaAs and InP. Nowadays deep-submicron CMOS transistors already achieve high performance which make them capable to handle 40 Gb/s signals in future products.

Typically, high-speed MUX circuits use current-mode logic (CML) with differential signals. Compared to conventional static CMOS logic CML allows a reduction of the internal voltage swing. The CML-circuit technique is a must for high-speed applications. The lower internal voltage swing is essential for high switching speeds. The basic concept of CML-circuit technique consists of series gating (stacked circuit architecture). Common CML designs have three or more gates in series which implies to have enough supply voltage for correct functionality.

In future CMOS technologies the threshold-voltage of the MOS-devices does not scale with the same factor as the supply voltage. This fact let the designer run in problem when using the conventional CML-technique. Aim of the work presented here was to realize a 2:1 MUX with focus on high-speed while using low supply voltage.

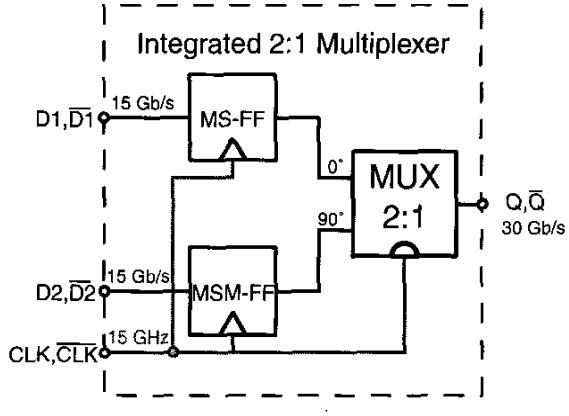

Fig. 1. Top-level block diagram of the monolithic transformer coupled 2:1 data multiplexer.

II. Circuit Design

The monolithic transformer coupled 2:1 MUX IC (Fig. 1) consists of a master-slave flip-flop (MS-FF), a master-slave-master flip-flop (MSM-FF) and the 2:1 multiplexer (MUX 2:1). The inputs of the MUX IC are

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two in-phase differential 15-Gb/s data signals, D1 and D2. Full-rate data aquisition is done by the MS-FF and MSM-FF (f_{CLK} = 15 GHz). The desired phase shift of 90 degrees between the MUX 2:1 inputs is achieved by adding an extra latch in series to one path (MSM-FF). Finally, the data streams D1 and D2 are multiplexed by the MUX 2:1 to a 30-Gb/s data stream. The MUX uses no output buffer.

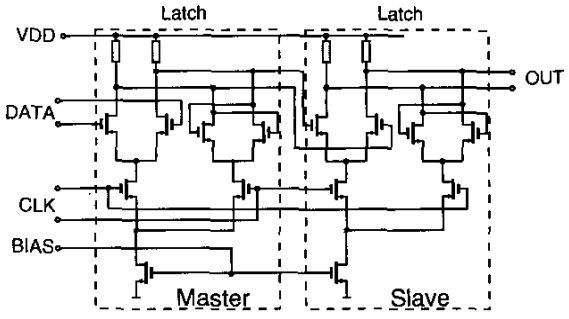

Fig. 2. Schematic diagram of the MS-FF.

The MS-FF (Fig. 2) consists of two latches connected in series. All nMOS transistors in the core are low-V_t 0.12μm nMOS devices. The latches use series gating between clock and data inputs. All data path transistors are of the same size and are 3/5 the width of the clock transistors. Poly-silicon resistors are used as load. One latch consumes 4 mA at 1 V supply. Clock input matching is realized with 100-Ω on-chip resistors, which are connected to a DC level shifter (VDD/2).

A. MUX 2:1 Circuit

Fig. 3 shows the schematic diagram of the monolithic transformer coupled MUX stage. The transformer splits the conventional CML-MUX design into the MUX-Core and the MUX-Clock section. The clock is the only signal in the MUX which is no broadband signal. We can take advantage of this fact and use a monolithic transformer to couple the clock signal from the MUX-Clock to the MUX-Core (Fig. 3).

There are outstanding advantages due to the on-chip transformer. Because of the missing DC-path between primary and secondary side of the transformer the MUX-Core and the MUX-Clock section can use the full supply voltage. The effective supply voltage for the MUX 2:1 circuit is doubled. The supply voltage of MUX-Core and MUX-Clock is connected to the center taps of the monolithic transformer. In this circuit are only two gates in series while using the full supply voltage.

The input-transformer X1 is connected as a parallel resonant device. The MOS capacitors C are connected in parallel to the primary windings of the transformer. The

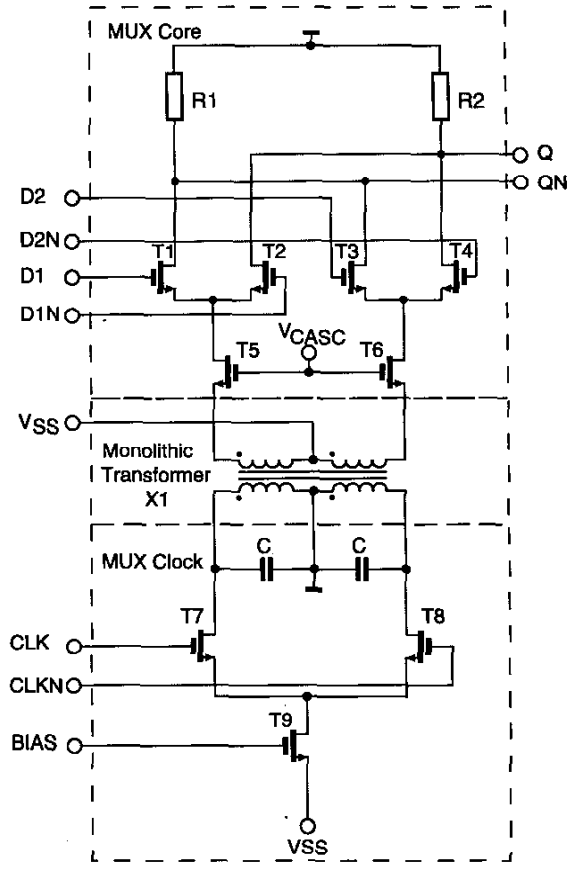

Fig. 3. Schematic diagram of the multiplexer stage with the monolithic transformer.

resonant tuning increases the current transfer ratio of the transformer. The cascode transistors $T5$ and $T6$ provide isolation between the data-path transistors $T1$-$T4$ and the transformers parasitic capacitances. All transistors of the MUX stage are nMOS devices because of their higher speed compared to pMOS transistors. Except for the current-source transistors low-V_t devices with gate lengths of 120nm are used everywhere. The MUX stage uses 70 Ω poly-silicon load resistors which is a compromise between high voltage swing and reasonable output matching. The tail current is set to 5 mA. The DC level of the sinusoidal clock signal is VDD/2.

B. Transformer Design

Fig. 4 shows the schematic symbol and the layout of the monolithic transformer. The transformer X1 consists of two primary turns and two secondary turns. The turn ratio is $N = 2:2$. Both windings have a center tap available. The upper two metal layers are connected in

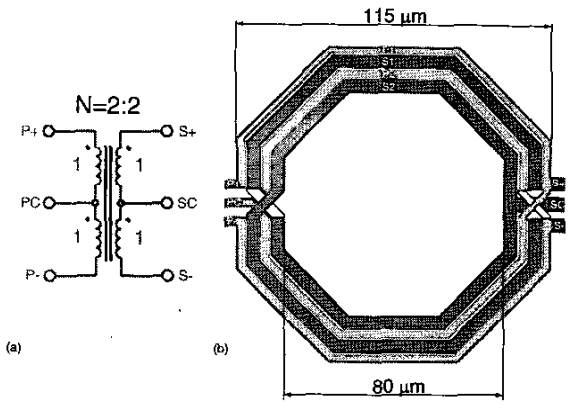

Fig. 4. Monolithic transformer X1: (a) Schematic symbol (b) Layout (Outer diameter: 115 μm).

parallel to decrease ohmic loss. The outer diameter is 115 μm and the inner diameter is 80 μm. The lateral spacings between the turns is 0.5 μm. The conductor-width is 5 μm of each primary turn and 3 μm of each secondary turn.

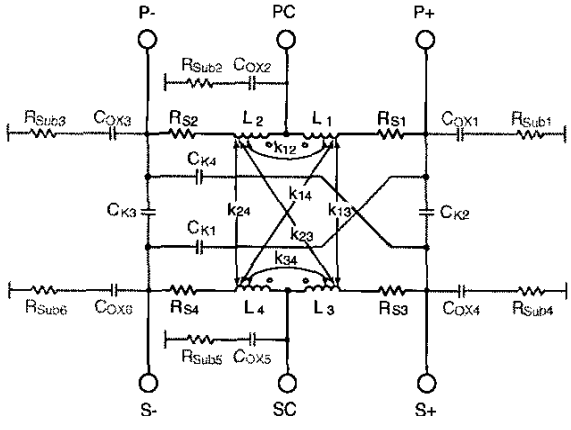

Fig. 5. Equivalent circuit of an on-chip transformer with primary and secondary center taps.

A lumped low-order model, shown in Fig. 5, of a transformer can be derived from the transformer geometries. The modeling of monolithic transformers is described in [7]. The following basic elements of the equivalent circuit can be identified:

- Multiple coupled inductors of the windings.
- Ohmic loss in the conductor material.
- Parasitic capacitive coupling between the windings.
- Parasitic capacitive coupling into the substrate
- Substrate loss

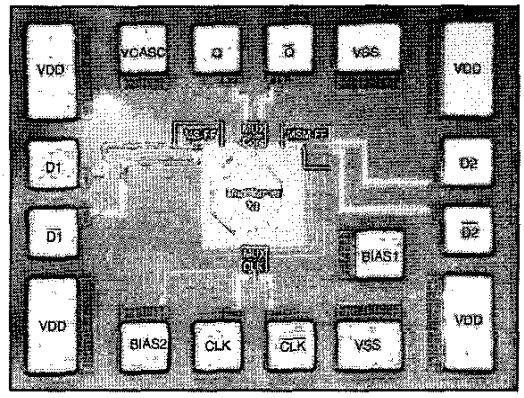

Fig. 6. 2:1 MUX chip micrograph (Size: 0.63x0.47 mm^2).

The clock transfer function from MUX-Clock to the MUX-Core is based on a high current transfer ratio of the on-chip transformer. In contrast to an ideal transformer the current transfer ratio of a lossy transformer is not equal to the value of the turn ratio. As shown in [6], the absolute value of the current transfer ratio of an ideal, but lossy tuned, transformer is $I_p/I_s = k \cdot Q \cdot \sqrt{L_p/L_s}$, where Q is the loaded quality factor, L_p and L_s is the inductance of the primary and secondary winding and k is the coupling coefficent. A high k and a high Q, for a given L_p and L_s, results in a high current transfer ratio.

III. Technology

The ICs are fabricated in a 0.12μm CMOS technology with six-layer copper metallization [8]. The manufactured nMOS transistors have a cut-off frequency f_t of 100 GHz and a maximum oscillation frequency f_{max} of 50 GHz. The MUX has a chip size of 0.63x0.47mm^2, which is determined by the pad frame. Fig. 6 shows a chip micrograph of the MUX.

IV. Experimental Results

For measurement the 2:1 MUX IC is mounted on a 30x30mm^2 0.51-mm RO4003 microwave substrate with SMA connectors. The measured data represents the performance of the ICs including the loss due to bond wires, microstrip lines on the test board and RF connectors.

The multiplexer is tested with two differential pseudo-random signal generators (PRG) which have a sequence length of 2^7-1. The input voltage swing is 2x400mV$_{pp}$ on 50 Ω at the SMA connectors. The sinusoidal clock signal has a voltage swing of 2x450mV$_{pp}$. Fig. 8 shows the measured eye diagram of the differential output signal at a data rate of 30 Gb/s. The measured eye opening is 2x100mV at 50 Ω load. The 2:1 MUX draws 28 mA at 1 V. Table I summarizes the features of the 2:1 MUX IC.

Function	2:1 MUX
Technology	120 nm CMOS, f_t=100 GHz
Chip size	0.63x0.47mm^2
Supply voltage	-1 V
Max. output bit rate	30 Gb/s
Current consumption	28 mA
Power dissipation	28 mW

TABLE I. Summary of the 2:1 MUX IC.

V. Conclusion

We have presented a fully integrated low-voltage 2:1 multiplexer in 0.12μm standard CMOS. This new circuit technique allows very low supply voltages, which is the trend of future CMOS technologies, while achieving very high operating speeds. The MUX works with a supply voltage down to 1 V at a data rate of 30 Gb/s. Up to now this is the highest operating speed reported for a 2:1 MUX working from 1 V supply voltage.

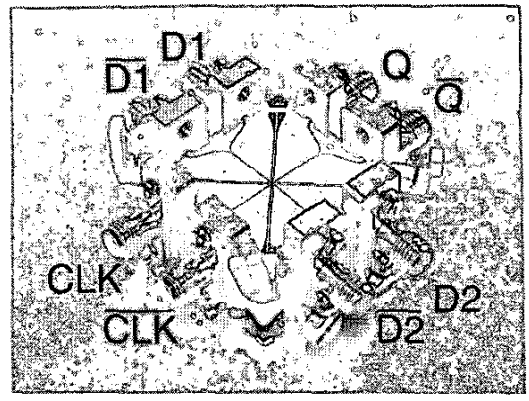

Fig. 7. 2:1 Multiplexer high-frequency test fixture (30x30 mm^2).

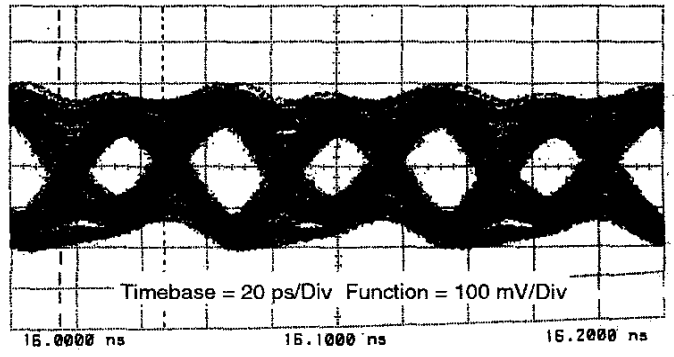

Fig. 8. Measured eye diagram of multiplexer output (30Gb/s, differential signal).

References

[1] H. Knapp, H.D. Wohlmuth, M. Wurzer and M. Rest, "25 GHz Static Frequency Divider and 25 Gb/s Multiplexer in 0.12μm CMOS", in *IEEE International Solid-State Circuits Conference*, pp. 302–303. IEEE, 2002.

[2] M. M. Green, A. Momtaz, K. Vakilian, X. Wang, K.C. Jen, D. Chung, J. Cao, M. Caresosa, A. Hairapetian, I. Fujimori and Y. Cai, "OC-192 Transmitter in Standard 0.18μm CMOS", in *IEEE International Solid-State Circuits Conference*, pp. 248–249. IEEE, 2002.

[3] J. Cao, A. Momtaz, K. Vakilian, M. M. Green, D. Chung, K.C. Jen, M. Caresosa, B. Tan, I. Fujimori and A. Hairapetian, "OC-192 Receiver in Standard 0.18μm CMOS", in *IEEE International Solid-State Circuits Conference*, pp. 250–251. IEEE, 2002.

[4] J. R. Long and M. A. Copeland, "A 1.9 GHz Low-Voltage Silicon Bipolar Receiver Front-End for Wireless Personal Communications Systems", *IEEE of Solid-State Circuits*, vol. 30, n. 12, pp. 1438–1448, Dec 1995.

[5] A. Heinz, W. Simbürger, H.D. Wohlmuth, P. Weger, W. Wilhelm, R. Gabl and K. Aufinger, "A Monolithic 2.8V, 3.2W Silicon Bipolar Power Amplifier with 54% PAE at 900MHz", in *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 117–120, Boston, June 2000.

[6] W. Simbürger, H.D. Wohlmuth and P. Weger, "A Monolithic Transformer Coupled 5W Silicon Power Amplifier with 59% PAE at 0.9GHz", *IEEE Journal of Solid-State Circuits*, vol. 34, n. 12, pp. 1881–1892, Dec 1999.

[7] D. Kehrer, W. Simbürger, H.D. Wohlmuth and A.L. Scholtz, "Modeling of Monolithic Lumped Planar Transformers up to 20 GHz", in *Custom Integrated Circuits Conference*, pp. 401–404, San Diego, May 2001, IEEE.

[8] T. Schiml et al, "A 0.13μm CMOS Platform with Cu/Low-k Interconnects for System On Chip Applications", in *VLSI Technology Digest of Technical Papers*, pp. 101–102. IEEE, 2001.